1. The register which has the data for the memory unit is termed as the MBR
2. PC has......... Address of the instruction
3. How many instructions can be fetched during one memory access in IAS? 2
4. what will be the minimum size of the address bus if 1Mega main memory is interfaced with the computer 20
5. In --- IO mechanism, same instruction is used for memory and IO read operations Memory mapped IO
6. Base 'b' systems has a digit 'x'. What is the remainder of x/b? x
7. Choose the best answer: When the fractional of an octal number is multiplied by 8, the integer value is: 5
8. The decimal equivalent of the hexadecimal number 1.2 is 16.125
9. The octal equivalent of the decimal number 11.2 is 13.14
10. The binary equivalent of the octal number 27.3 is 10111.11
11. The hexadecimal equivalent of the binary number 1011110.11001 is 5E.C8
12. The range of 2's complement representation with 5 bits is (-16) to (+15)
13. Add in 4 bit 2's complement: 1000+1111=? (in decimal) (+7)
14. The 2's complement representation of (-7) is 11111001
15. The decimal equivalent of the 2's complement number 1111111111111101 is: -3
16. In the binary multiplication ---, ---- and ---- bits are shifted right. Choose the correct order. C,A,Q
17. "If the pattern ""1011"" is arithmetically shifted right, then the result is: (omit the leading zeroes)" 1101
18. During binary division which operation is not performed? Arithmetic shift right
19. When subtracting (-5) from (+4) in 4 bit 2's complement representation, the result is: 1
20. The value of (0001) is --- in signed magnitude,--- in 1's complement and --- in 2's complement {+1,+1,+1}
21. In relative addressing mode, the effective address is \_\_\_\_\_\_ PC content + address
22. PUSH is an example for \_\_\_\_\_\_ address instruction zero
23. A simple instruction has 4 bits for opcode, 6 bits for source operand and 6 bits for destination operand and no bit(s) is(are) reserved for future enhancement. It implies that the processor can perform \_\_\_\_ different operations. Pick the suitable one from the options 12
24. RISC processor has \_\_\_\_\_\_ Few addressing modes
25. MBR content is moved to \_\_\_\_\_ during interrupt and to \_\_\_\_\_\_\_ during indirect and to \_\_\_\_\_\_ during \_\_\_\_\_\_ during fetch respectively in the instruction cycle PC, MAR, IR
26. Which policy of superscalar is usually faster? Out of order issue;out of order completion
27. Antedependency is \_\_\_\_\_\_\_ Read after write
28. Which type of instruction is needed to do the following task? The entered key from keyboard is moved to register A by the processor Input-Output
29. The PC content is altered by the during \_\_\_\_\_\_ instruction Branching
30. MBR is \_\_\_\_\_\_\_ Memory Buffer Register
31. In register addressing mode, the effective address is\_\_\_\_ Register
32. Which type of instruction will do the given task? A data has to be moved to register R1 if carry is 1; Else it has to be moved to register R2. Data transfer
33. Instruction set has collection of all \_\_\_\_\_\_\_ Instructions
34. Consider the stack of a hypothetical 8 bit processor begins from the address 0x7fffffff; the current top of the stack is 0x7fffffff4. After using 2 PUSH and 3 POP operations, the top of the stack will be \_\_\_\_\_ 0x7ffffff5
35. To reset bit-5 of a 16 bit instruction without affecting other bits, \_\_\_\_\_\_ operation is used OR
36. The decimal value for the given EBCDIC \_\_\_\_\_\_\_ is \_\_\_\_\_\_\_ and its ASCII value is \_\_\_\_\_\_\_ 11110011, 3, 0110011
37. Instruction cycle begins with \_\_\_\_\_ and end with \_\_\_\_\_\_ Instruction Address Calculation, Operand store
38. Say true (T) or false (F): The above 3-stage pipelined processor' s performance can be enhanced by making the second stage execution time as 0.5 from 2 F
39. CISC stands for \_\_\_\_ Complex Instruction set computer
40. Say true (T) or false (F): PC content is incremented twice during indirect addressing mode F
41. CD ROM is \_\_\_\_\_ memory optical
42. Consider a 16M bit memory is organized as 4M memory locations. Then a single memory location has \_\_\_\_ bits of data 4
43. Register memories are \_\_\_\_ than magnetic tape memories costiler and smaller
44. Normally, SRAM has \_\_\_ transistors 6
45. T1 is the access time of L1 memory and T2 is the access time of L2 memory. T2 = 100 \*T1. If T2 is 1 microsecond and the hit percentage is 95, what is the total access time to execute 1000 instructions? Ignore the time of moving the data from L2 to L1 during miss. 59.5 microsec
46. Memory access time is \_\_\_\_\_ memory cycle time less than
47. A cache can hold 16KB data and the main memory size is 16MB. A line has 32 bits of data. A 24 bit address locates a byte of data in main memory. How many bits are allocated for tags in a fully associative mapping? 22
48. Pick the pointing device Mouse
49. Busy waiting is used in \_\_\_\_ IO Programmed IO
50. Raster scan provides the refreshing rate \_\_\_ frames per second 72
51. The \_\_\_\_\_ access technique wastes most of the processor cycles Programmed IO
52. Choose the best answer. What is the objective of inline functions in C++? Optimize time and space
53. The \_\_\_\_ memory is only once writeable PROM
54. Throwing one page when another page is brought is called as \_\_\_ Page replacement
55. The \_\_\_\_\_ technique does not differentiate odd and even lines when refreshing non-interlaced
56. xerographic printing process is used in \_\_\_ Laser printer
57. CD ROM is \_\_\_- memory Optical
58. Consider a 16M bit memory is organized as 4M memory locations. Then the address has \_\_\_ bits 22
59. Say true(T) or false(F) if possible from the given data. The size of the address bus decides the size of virtual memory F
60. Consider a 16KB Cache and 16MB main memory. A block of main memory has 32 bits of data. The first block is named as b0 and the first address is byte 0. The cache uses 2 bits for word field.Direct mapping is followed in the memory organization. On which cache line the main memory byte 1067 will be mapped? Line 266